

PICOTDC

The PicoTDC is a specially developed 64 channel Time to Digital Converter (TDC) ASIC in 65nm CMOS for use in High Energy Physics (HEP) experiments and similar scientific applications where high rate, very high time resolution single shot time measurements are required on a large number of channels. It is a successor to the HPTDC chip that over the last 15 years has been used extensively within HEP and other domains.

FEATURES

- 3ps or 12ps binning with very low jitter (<1ps) and high stability (~1ps).
- 40MHz reference clock to which all time measurements are locked via PLL and DLL.
- 64 or 32 differential channels.
- Leading / trialing edge mode or leading edge plus TOT mode.
- Large on-chip data buffering capability.
- Option of triggering with programmable latency and time window.
- Support for overlapping trigger windows.
- Option of using channel 0 as timing channel and trigger generator channel.
- 1 or 4 8bit readout ports at 320MHz.
- 3/12ps resolution test pulse generator.
- I2C control and monitoring interface.

APPLICATIONS

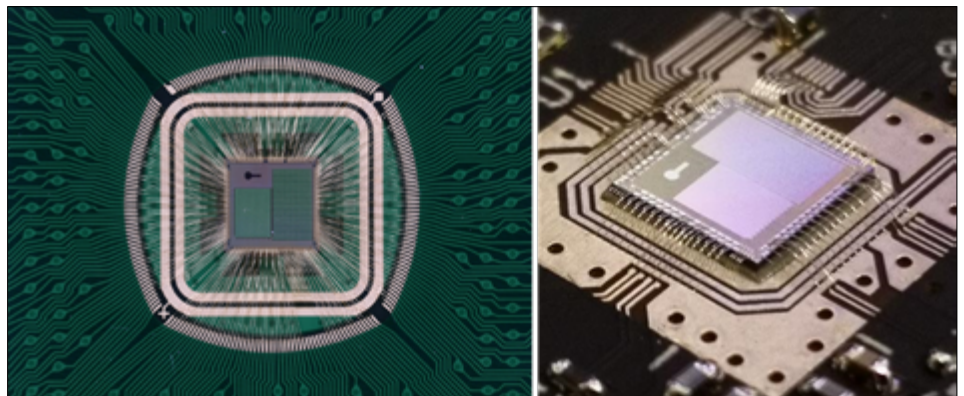
High performance time to digital converter ASIC chip for use in applications requiring precise time-tagging of electronic signals, e.g. for electron and photon detection in medical imaging, laser ranging, life science, material research or scientific instrumentation. This so-called pico-TDC ASIC allows precise time-tagging of up to 64 input channels relative to an external clock reference of 40MHz.

AREA OF EXPERTISE

Microelectronics

CONTACT PERSON

aurelie.pezous@cern.ch
Find out more at: kt.cern



Picture of the PicoTDC chip. (Image: CERN)



technology

Knowledge Transfer
Accelerating Innovation