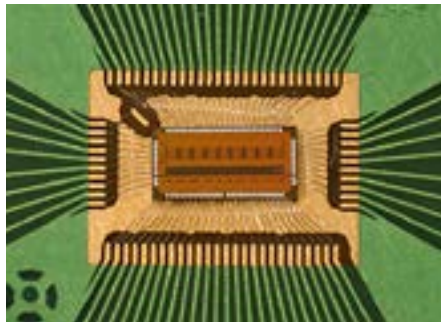


# NINO



*CERN has available a low power front-end amplifier discriminator ASIC chip for use in applications based on electron and photon detecting in medical imaging, life science or material research. This NINO ASIC allows for an 8-channel input signal charge measurement through encoding discriminator pulse width with excellent timing resolution at very high rate, while at the same time providing a very low noise performance and power consumption characteristics per channel.*

*At CERN, this technology is used for time-of-flight measurements for particle vertex reconstruction in the ALICE experiment of the LHC collider.*

## AREA OF EXPERTISE

- Electronics

## FEATURES

- Compact packaging through 0.25 $\mu$ m CMOS technology (fits in a 2x4 mm<sup>2</sup> area).
- Adjustable discriminator thresholds.
- Adjustable 50 ohm input resistance.
- 27mW power consumption per channel.
- Front-end time jitter <10ps.
- Sustains very high rate (>>10MHz).
- Channels: 8.
- Voltage supply: 2.5V.
- Peaking time: 1ns.
- Input signal range: 30fC - 2pC.
- Noise: <2500 e<sup>-</sup>.
- Discriminator threshold: 10fC - 100fC .
- Timing precision: <10ps jitter.
- Output: LVDS.

## CONTACT PERSON

[aurelie.pezous@cern.ch](mailto:aurelie.pezous@cern.ch)

Find out more at:

[kt.cern](http://kt.cern)

## APPLICATIONS

- Photon and electron detection at very high rates in medical imaging, life sciences and material research.

## IP STATUS

- Produced in 0.25 $\mu$ m CMOS technology, the NINO ASIC is available off-the-shelf for licensing or can be produced on short term.
- Upon request, CERN provides support and pre-configured solutions (data acquisition, chip boards, readout software) for the integration of such chips with user specific detectors and mechanical support structures.



