# HIGH PERFORMANCE TIME TO DIGITAL CONVERTER

## AREA OF EXPERTISE

- Electronics

## IP STATUS

- Fully developed product ready for licensing. Small quantities of the HPTDC ASIC are available off the shelf from CERN in combination with an exploitation license. Larger quantities may be produced on short term. Upon request, CERN can provide support for the integration of such chips within user specific applications.

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Find out more at:
kt.cern

***This technology is a high performance time to digital converter ASIC chip for use in applications requiring precise time-tagging of electronic signals, e.g. for electron and photon detection in medical imaging, laser ranging, life science or material research. This so-called HPTDC ASIC allows precise time-tagging of up to 32 input channels relative to an external clock reference of 40MHz. Based on an integrated clock multiplying Phase Locked Loop (PLL), a 32-channel Delay Locked Loop (DLL) with integrated RC-delay lines provides time interpolation down to 25ps.***

***At CERN this technology is widely used in high resolution mode in time-of-flight particle detectors in LHC experiments (ALICE TOF) and in low resolution for drift based muon detectors (CMS DT) and a multitude of other experiments at CERN (NA48) and outside CERN (STAR, BES, OKU, KABES, HADES).***

## FEATURES

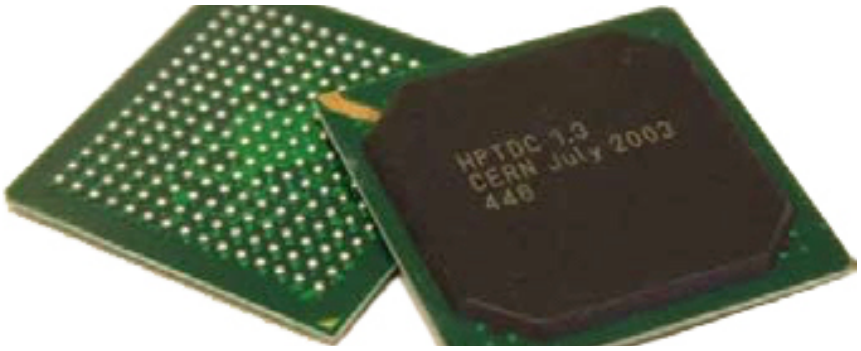
- Time solution programmable from 25ps to 800ps.
- Between 8 and 32 channels per chip available.
- Low data volume through event triggered data processing (no continuous data sampling).

## APPLICATIONS

- Signal processing in instrumentation for biology, medical imaging, laser ranging, life sciences and material research.

## PLANNED DEVELOPMENTS

- Produced in 0.25µm CMOS technology. 32 input channels. Programmable time resolution between 25ps to 800ps.

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